OSIRIS project, a Research and Innovation Action (RIA), started on May 1st 2015. The objective is to substantially improve the cost effectiveness and performance of gallium nitride (GaN) based millimetre wave devices. It elaborated innovative SiC materials using isotopic sources in order to reach thermal conductivity improvement of 30% which is important for SiC power electronics and microwave devices using GaN high electron mobility transistors (HEMT) grown on SiC semi-insulating substrates. The improved thermal SiC properties will be obtained by using single isotopic atoms for silicon and carbon, namely $^{28}\text{Si}$ and $^{12}\text{C}$. The SiC wafer size will be targeted to 100mm (4-inches) which is today widely used in industry. For microwave GaN/SiC HEMT, this isotopic approach should create a complete shift in the currently used SiC substrate/GaN epi-wafer technology by growing the high thermal conductivity (+30%) semi-insulating SiC on top of lower cost semiconducting SiC substrates. The project will evaluate HEMT microwave power performance improvement at 30GHz thanks to better thermal environment. For power electronics, this innovation will be essentially focused on thermal improvement not on price fall, i.e. better electron mobility at a given power dissipation as mobility and drift mobility decrease with temperature and also better carrier transport thanks to lower scattering rates. Schottky and p-i-n diodes will be tested using this material.
OSIRIS quantitative objectives are based on initial thermal simulations for the two targeted applications:

I. Microwave applications
- Potential cost of processed wafer: decrease of 30%
- Thermal resistance improvement: 5°C.mm/W for 20 mm total gate development
- Lifetime: improvement by around 1 order of magnitude
- Microwave gain: increase of 1dB
- Electrical efficiency: increase of about 5% for high frequency CW applications

II. Power electronics applications
- Planar device: Thermal resistance improvement of 5°C.mm/W for 100 mm gate width.

III. OSIRIS Partnership

OSIRIS Partnership includes six companies and three public institutions from four European countries: France, Norway, Slovakia, and Sweden.

Project Leader : Sylvain Delage; III-V Lab (sylvain.delage@3-5lab.fr)
Dissemination : Pierre Ruterana ; CIMAP (pierre.ruterana@ensicaen.fr)
Website : http://osiris-ecselju.eu/
IV.1. LiU:
- SiC epitaxial growth
- SiC vanadium doping
- SiC thermal conductivity

IV. 2. ISOSILICON
- Synthesis of isotopic Si.

IV. 3. Ascatron: Evaluated of the diodes produced on isotope pure and natural material.

IV. 4. III-V Lab:
- Growth of quaternary InAlGaN/GaN HEMT on natural and isotopic epitaxial SiC.
- Fabrication of 0.15µm gate length HEMT using InAlGaN/GaN grown in our lab and AlGaN/GaN grown by Linköping University.
- Electrical characterisation exhibited up to 10W mm\(^{-1}\) output power at 30GHz in CW using quaternary structures.
- Thermal characterisation using infrared microscope of PiN ASCT diode.

IV. 5. STUBA:
- Development of a Thermal chuck for electro-thermal characterization
- Electro-thermal characterization and simulation of HEMT devices

IV. 6. Intraspec technologies:
- Development of analysis techniques for HEMT devices

IV. 7. CIMAP
- Modeling of materials stability
- Local structure and chemistry in HEMT devices

IV. 8. Norstel: Wafer processing for epitaxial growth

IV. 9. UMS
- Complementary microwave characterisation of III-V Lab 0.15µm HEMT
- Support to HEMT packaging for thermal and electrical characterization
IV.1. Linköping University

SiC epitaxial growth

- The growth process for thick (100 µm) Vanadium doped semi-insulating SiC epi on 4” on-axis SiC substrates was further developed and optimized
- Significant improvement with respect to surface morphology and 3C-inclusions

Vanadium doped SiC

- High concentrations of V lead to V-precipitate like defects triggering the formation of 3C-SiC
- Reduction of V-precursor flow rates to levels where these defects do not appear can still give high resistivity
- Highly resistive epilayers free of 3C, with room temperature resistivity better than 2x10⁸ Ω-cm was achieved

Measurement of SiC thermal conductivity

- Thermal conductivity measured by transient thermo-reflectance method

<table>
<thead>
<tr>
<th>sample</th>
<th>k (W/m K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nat. SI substrate</td>
<td>368</td>
</tr>
<tr>
<td>Nat. SI epi</td>
<td>361</td>
</tr>
<tr>
<td>Isotope SI epi</td>
<td>420</td>
</tr>
<tr>
<td>Nat. N+ substrate</td>
<td>322</td>
</tr>
<tr>
<td>Nat. N+ epi</td>
<td>289</td>
</tr>
<tr>
<td>Isotope N+ epi</td>
<td>350*</td>
</tr>
</tbody>
</table>

* estimated

Optical image taken from 100 mm wafer with over 100 µm thick SI epilayer grown under optimized growth conditions.
IV 2. ISOSILICON

The commercial development of semiconductor materials (e.g. SiC) improved by isotopic purity calls for a European, cost efficient, independent and reliable source of isotopes. So does the European quantum computing program, which in the years to come will need kilograms of $^{28}$Si at 99,99% isotopic purity. During the OSIRIS project, Isosilicon has tested new proprietary chromatographic column materials, operating in suitable industrial conditions of temperature and flow-rate as well as methods for the detection of scarcely noticeable behavior from one isotope to the other.

High performance Quadrupole Time Of Flight (QTOF) Mass Spectrometer (Agilent) for the detection of isotopes

Using the experimental data and the mathematical models developed through OSIRIS we find that the chromatographic method could support the commercial development of isotopic pure SiC semiconductors with a production of 100 kg 99% $^{28}$Si at a cost of 25 €/g by 2022.
IV 3. ASCATRON

Ascatron has evaluated the SiC diodes made on isotope pure and natural material as reference. State-of-the-art performance was achieved for the 10kV PiN diodes with a very low forward voltage drop due to high quality SiC material.

Comparison of forward voltage drop (upper) and minority carrier life-time (lower) of processed 10 kV PiN diode. Almost identical electrical performance could be demonstrated for both natural and isotope pure material. The forward voltage drop of 3.6 V at current of 220 A/cm² is very low for a device blocking 14 kV. Life-time measurements were done with Open Circuit Voltage Decay (OCVD) method by CTU Prague. Life-time values of 4.5 µs is proof of high quality material with low rate of point defects.

To reduce the switching losses without increasing conduction losses, proton radiation was used to locally decrease the minority carrier life-time, and by this limit the reverse recovery current at turn-off.

Custom designed packages for 10 kV diodes were developed to enable measurements and system demonstration in open air.

Performance of the PiN diodes is optimized for flue gas cleaning application. By replacing serial coupled 1 kV Silicon diodes with 10 kV SiC diodes in the high voltage rectifier of the transformer, the losses and size of the transformer can be reduced more than 50%. System demonstration is done in a project together with General Electric and supported by MISTRA in Sweden.
IV 4. III-V Lab

- Main objective for III-V Lab was to evaluate the compatibility of natural and isotopic epitaxial SiC wafer with GaN HEMT growth and process. This was supported by material analysis, electrical characterization and robustness.
- No major differences for the epitaxial growth of InAlGaN/GaN heterostructures have been observed.
- Device processing was also quite close for reference plain SiC wafers, natural and isotopic epitaxial SiC substrates, providing less mature wafers is taking into account.
- In the frame of OSIRIS project first bi-layer SiN and Al2O3 passivation was developed leading to more robust devices compared to former SiN passivation.
- Additional work would have to carried out to take advantage of the isotopic SiC layer.
- As a conclusion, state of the art has been obtained using Norstel/Linköping materials, but we could not yet discriminate between natural and isotopic materials.

Comparison of OSIRIS (Red stars with blue dot) wafer performances at CW 30GHz with best reported published results.
IV 5. STUBA

STUBA activities in OSIRIS have included thermal chuck development for electro-thermal characterization, micro-Raman, IR camera and DLTS measurements and electro-thermal simulation.

1. Thermal chuck for electrothermal characterization

A new heat sink plate, driving circuits and temperature controller have been developed. It is equipped with a precise Peltier temperature control and driving system for high power electro-thermal properties measurements through a micro-Raman system and a high resolution camera with 25 µm spatial resolution utilizing close up IR lens.

2. Electro-thermal characterization and simulation of HEMT devices

The temperature distribution across the GTLM HEMT region are measured by micro-Raman spectroscopy and compared with simulation results.

Simulated temperature distribution and infrared thermal image across a GTLM HEMT of packaged chip.
IV 6. Intraspec Technologies

1. Cathodoluminescence

In complement to SEM Catho-emission shows lack homogeneity in the material.

2. Electrical characterization

The measurements ($I_{ds}$-$V_{ds}$) carried out on OSIRIS devices allowed us to finalize and optimize the characterization bench and technique and by now, we are confident on our equipment as we systematically obtain stable and repeatable I-V measurements.

3. Ongoing development

That tool we are developing will allow us to execute an automated cross-sections series in a zone of interest as could be the volume under the whole gate finger or even the overall transistor. A series of cross-sections, spaced about 10nm from each other, produces many images that will be assembled to reconstruct the device virtual volume thanks to a dedicated software.
Through OSIRIS, the PM2E Team of CIMAP has developed two activities: 1. Our theoretical modeling of the alloys in WP2 allowed to show that at the growth temperatures and composition range for HEMTs barriers, the quaternary alloys should show a good thermal stability, in contrast to the ternary InAlN.

The spinodal behaviour of the quaternary InAlGaN alloys calculated as shown for different In compositions. The growth temperature is around 870°C (Horizontal black line).

2. Local structure and chemistry down to atomic scale. To this end, the TEM sample preparation FIB has been extensively deployed in order to fabricated highest quality thin lamella in cross section and plan view with an accurate localization at areas of interest in the HEMT devices.
After the SiC epitaxial growth at Linköping, the layers have been successfully planarized and thinned to target thickness by backgrinding. In particular, for the wafers with isotope pure layers, the challenge has been to keep wafer breakages at zero due to the limited availability. For the second half period of the OSIRIS project, no wafers has been lost due to planarization processes. More importantly, after our CMP process, all the wafers surface exhibited a roughness (RMS) <2Å for both off-axis and on-axis wafers. In this process, we delivered all the forecast wafers to Linköping University, III-VLab and Ascatron for the next steps.

100 mm semi-insulating state of the art substrate from Norstel. These substrates are used as bench mark in the device processing and evaluation.
## Key results of OSIRIS project

- Isotopic separation has been studied and suitable $^{28}$Si separation was determined at lab scale.
- Excellent SiC epitaxial layers were obtained on off-axis SiC substrates with high electrical resistivity.
- Development of high quality SiC epitaxy on to of on-axis substrates without 3C inclusion.
- High electrical resistivity of on-axis SiC epilayers and tailored resistivity for PiN and Schottky diodes with or without isotopic SiC.
- Isotopic thermal conductivity: Following initial value obtained by Linköping University, thermal characterisation showed an improvement of 20% instead of the initially foreseen 30%.
- The full chain of metrology has been successful and a very good coherence was obtained between thermal conductivity assessment by Transient Thermo-Reflectance, device thermal characterisation by Raman spectroscopy as well as Infrared microscopy with electrothermal simulations.
- Device processing shows that the new epitaxial SiC material is compatible with SiC diodes and GaN HEMT.
- Osiris objectives have been fulfilled. Additional work will have to be undertaken for industrialisation.

<table>
<thead>
<tr>
<th></th>
<th>Natural SiC PiN diode</th>
<th>PiN diode including isotopic epilayer but with natural SiC substrate</th>
<th>Fully isotopic PiN diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rth_top-bottom</td>
<td>1.17 °C/W</td>
<td>1.019 °C/W</td>
<td>0.971 °C/W</td>
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<tr>
<td>Rth_improvement</td>
<td>Reference</td>
<td>-13%</td>
<td>-17.1%</td>
</tr>
<tr>
<td>compared to natural SiC</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Thermal resistance of Ascatron PiN diodes based on experimental thermal resistance data and thermal simulation from STUBA.
A. OSIRIS Meetings: 5. Two years meeting at Ascatron, 29 June 2017 Kista; 6. Thirtieth months meeting in Bratislava, 15 December 2017; 7. Thirtieth Month meeting in III-V Labs, Palaiseau.

Members of OSIRIS present at the eighteenth Month meeting in UMS Villebon, from left to right:

B. OSIRIS Second Workshop
1. Workshop on devices and applications, December 14th 2017 at Slovak University of Technology, Faculty of Electrical Engineering and Information Technology in Bratislava

C. Upcoming events of interest to OSIRIS
1. Final meeting at III-VLab, Palaiseau, 27-28 November 2018